Substitute form 1449A/PTO				Complet if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	To Be Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Robert H. Bishop
				Group Art Unit	
(use as many sheets as necessary)				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	5646-98

U.S. PATENTS AND PATENT PUBLICATIONS

Examiner Initials*	Cite No.	U.S. Patent Document Number	U.S. Patent Document Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
	1	US-6,001,661		McBean, Sr.	12/14/1999
	2	US-5,859,474		Dordi	01/12/1999
	3	US-4,852,016		McGehee	07/25/1989
		US-			
		US-			
		US-			
		US-			
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.	Foreign Patent Document Office	Foreign Patent Document Number	Foreign Patent Document Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	T

OTHER NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
	4	Rörgren, *Chapter E: Ball Grid Array Technology*, The Nordic Electronics Packaging Guideline, 2000, 5 pp.	
	5	Horiuchi et al., *Escape Routing Design to Reduce the Number of Layers in Area Array Packaging*, IEEE Transactions on Advanced Packing, Vol. 23, No. 4, November 2000, pp. 686-691	
	6	Betz et al., *Effect of the Prefabricated Routing Track Distribution of FPGA Area-Efficiency*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 6, No. 3, September 1998, pp. 445-456	
	7	Wakabayashi et al., *An Optimal Pin Assignment Algorithm With Improvement of Cell Placement in Standard Cell Layout*, Proceedings of IEEE Asia Pacific Conference on Circuits and Systems '96, November 18-21, 1996, pp. 381-384	
	8	Greenberg et al., *Single-Layer Channel Routing and Placement with Single-Sided Nets*, Computers Math. Applic., Vol. 32, No. 4, 1997, pp. 1-7	
	9	Chen et al., *A Pin Permutation Algorithm for Improving Over-the-Cell Channel Routing*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, No. 8, August 1995, pp. 1030-1037	
	10	Li et al., *Global Routing for Gate Array*, IEEE Transactions on Computer-Aided Design, Vol. CAD-3, No. 4, October 1984, pp. 298-307	

Examiner Signature	Nitin Parekh	Date Considered	10/12/04

*EXAMINER: Initial if ref rence considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not consid r d. Include copy of this form with next communication to applicant.